NORTH MAHARASHTRA UNIVERSITY,

JALGAON (M.S.)

BACHELOR OF ENGINEERING (B.E.)
(FINAL YEAR)

ELECTRONICS ENGINEERING

TERM – I and II

W.E.F 2008 – 2009

NORTH MAHARASHTRA UNIVERSITY, JALGAON
STRUCTURE OF TEACHING AND EVALUATION
B.E. (ELECTRONICS ENGINEERING)
FIRST TERM

W.E.F. 2008-09

SR.No.	Subject	Teaching Scheme Hours / Week			Examination Scheme				
		Lectures	Tutorial	Practical	Paper Duration Hours	Paper	TW	PR	OR
1	Power Electronics - I	4	-	2	3	100	25	25	-
2	* Fiber Optic Communication	4	-	2	3	100	25	-	-
3	* Digital Signal Processing and Processors	4	-	2	3	100	-	25	-
4	* Computer Communication Networks	4	-	-	3	100	25	-	-
5	Elective - I	4	-	2	3	100	25	25	-
6	* Project - I	-	-	2	-	-	25	-	25
7	* Seminar	-	-	2	-	-	25	-	-
	Total	**20**		**12**		**500**	**150**	**75**	**25**
	Grand Total	**32**			**750**				

SECOND TERM

SR. No.	Subject	Teaching Scheme Hours / week			Examination Scheme				
		Lectures	Tutorial	Practical	Paper Duration Hours	Paper	TW	PR	OR
1	Digital Communication System	4	-	2	3	100	25	25	
2	Power Electronics - II	4	-	4	3	100	25	25	-
3	Process Instrumentation	4	-	2	3	100	25	-	-
4	Elective -II	4	-	2	3	100	25	25	-
5	* Industrial Visit / Case Study	-	-	-	-	-	25	-	-
6	* Project - II	-	-	4	-	-	100	-	50
	Total	**16**	**-**	**14**		**400**	**225**	**75**	**50**
	Grand Total	**30**			**750**				

* Common with B.E. (Electronics and Communication, Electronics and Telecommunication)

ELECTIVE I	i) * VLSI Design
	ii) Robotics
	iii) * Biomedical Instrumentation
	iv) Artificial Intelligence

ELECTIVE II	i) * Embeded System
	ii) * Digital Image Processing
	iii) * Neural Network and Fuzzy systems
	iv) * Nanotechnology

TERM - I
POWER ELECTRONICS –I

Teaching scheme:	**Examination scheme:**
Lectures: 4 hrs / week	**Theory Paper : 100 Marks (3 Hours)**
Practicals: 2 hrs / week	**Practical : 25 Marks**
	Term Work : 25 Marks

UNIT I
Power Devices: SCR – construction, two transistor analogy , operation , V - I characteristics , ratings, turn on and turn off dynamic characteristics, turn on and turn off times, turn on and turn off methods. **GTO** – basic structure, V - I characteristics, turn on and turn off operation, switching characteristics, inclusion of snubber and drive circuits. Turn on and turn off transients, minimum on and off state times, maximum controllable anode current, .over current protection. **IGBT** - basic structure , V - I characteristics , device operation, blocking state and on state operation, latching in IGBT, causes and avoidance of latch ups, switching characteristics, turn on and turn off transients. **MOSFET** - basic structure, V - I characteristics, inversion layers and field effect gate control of drain current , switching characteristics, switching waveforms , voltage break down , on state conduction losses. **FCT AND JFET**: construction and characteristics. **Lectures 10, Marks 20**

UNIT II
Line frequency phase controlled converter – **1-Φ converters** - 1-Φ bridge semi converter and full converter , R , R –L , R-L –E load, idealized circuit, dc side voltage and performance parameters, effect of Ls, discontinuous current conduction, inverter mode of operation. **3-Φ converters** - 3-Φ bridge semi converter and full converter, R, R –L load, idealized circuit, dc side voltage and performance parameters assuming highly inductive load, effect of Ls, inverter mode of operation. **Power factor improvement –** SAC and EAC. **Lectures 10, Marks 20**

UNIT III
Dc-Dc switch mode converters – block diagram, step up, step down converter, continuous and discontinuous mode of operation, boundary between continuous and discontinuous conduction, full bridge dc –dc converter with bipolar and unipolar PWM. Voltage switching, ripple in output voltage. **SMPS** – overview, control of SMPS, block diagram voltage feed forward PWM control, current mode control, digital PWM control, power supply protection, soft start, electrical isolation of feed back loop, designing to meet power supply specifications, synchronous rectifier. **Lectures 10, Marks 20**

UNIT IV
Switch mode dc to ac inventers – Parallel inverters, basic concept of switch mode inverters, PWM switching scheme, square wave switching scheme, single phase inverters, half bridge inverters, full bridge inverters, three phase inverters, PWM in three phase voltage source inverters, programmed harmonic elimination switching. **UPS** – Black diagram and description. **Lectures 10, Marks 20**

UNIT V
Resonant Converters – Zero voltage and / or zero current switching, switch mode inductive current switching, classification of resonant converters, - Undamped series resonant circuit – capacitor parallel load circuit, frequency characteristics, load resonant converters – SLR, PLR – Operation, steady state characteristics and control, current source parallel resonant dc-ac inverter for induction heating, class – E resonant converter, ZCS and ZVS Resonant switch converters. **Lectures 10, Marks 20**

References:
1. Ned Mohan, TM Undeland William P. Robbins - Power Electronics converters, Applications and Designs, John Wiley and sons, Edition 2nd
2. Mohammad M. Rashid - Power Electronics – circuits, Devices and Applications, PHI, Edition 2nd / Pearson
3. M. Rammamoorthy - Introduction to Thyristor and their Applications.
4. Singh and Khanchandani - Power Electronics , TMH, Edition 2nd

List of Practical:
1. Characteristics of devices: GTO / IGBT / Power MOSFET (**TWO** practical)
2. Line Commutated controlled converter (**TWO** practical)
3. Chopper (**TWO** practical)
4. Inverter (**TWO** practical)
5. Resonant Converter (**TWO** practical)

Note: Minimum **EIGHT** practicals are to be performed

NORTH MAHARASHTRA UNIVERSITY JALGAON
B.E. (ELECTRONICS, ELECTRONICS AND COMMUNICATION, ELECTRONICS AND TELECOMMUNICATION)

W.E.F : 2008- 09

TERM - I
FIBER OPTIC COMMUNICATON

Teaching scheme:	**Examination scheme:**
Lectures: 4 hrs / week	**Theory Paper: 100 Marks (3 Hours)**
Practical: 2 hrs / week	**Term Work : 25 Marks**

UNIT I
Introduction to Optical Fiber Communication System:
Block diagram of OFCS, Advantage and Disadvantage of OFCS over other communication systems. Ray theory of transmission and concept of acceptance angle and Numerical Aperture (Numericals based on this), Meridionial and skew propagate wave theory of optical propagation : cut – off wavelength. Group velocity and Group delay, Types of fibers (According to materials, Refractive index profile, Mode of propagation) Fiber Optic Splices, connectors, couplers, Directional Coupler. **Lectures 10, Marks 20**

UNIT II
Light Sources and Detectors:
Sources : Factors or Characteristics for their selection in OFCS, **Types :** Light Emitting diodes, Laser diodes, Surface emitter LEDS, Edge emitter LEDS, Super luminescent LEDS, LED operating Characteristics, **Modulation Bandwidth:** 3-dB electrical bandwidth, 3-dB optical Bandwidth, Radiation patterns of surface and Edge emitters, **Laser diode:** Laser principles, semiconductor laser diode , Hetero junction Laser , strip- gromentry lasers, Distributed feedback lasers, laser diode operating Characteristics, Radiation patterns.
Detectors: Characteristics or factors for their Selection, P-N photo diode, P-I-N Photo diode, Avalanche photodiode, detector parameters: Quantum efficiency, Responsivity, speed of Response (Numericals based on this)   **Lectures 10, Marks 20**

UNIT III
Modulation: Noncoherent / Coherent
Intensity Modulation: LED Modulation and Circuits (Analog and digital) Analog modulation formats; AM / IM Sub carrier Modulation, FM / IM Sub carrier Modulation. Digital Modulation formats; PCM: RZ, NEZ, Manchester, Bipolar codes, Other digital formats: PPM, PDM, OOK, FSK And PSK.
Detection: (Coherent detection / Heterodyne / Homodyne detection) :- Optical heterodyne receivers, Optic Frequency Division Multiplexing. **Lectures 10, Marks 20**

UNIT IV
Losses in fibers: Absorption, scattering and bending losses. Signal distortion in optical fiber: Material dispersion, waveguide dispersion, intermodal dispersion. Noise in optical fiber: Thermal Noise, shot noise, S / N Ratio, Noise equivalent power (Numericals based on this)
Fiber Optics System Design: Optical power budgeting, Rise-time budget.
Optical Fiber Measurements: Measurement of Attenuation, dispersion,   refractive index.   Field   Measurements: Optical time domain reflectometry. (OTDR) **Lectures 10, Marks 20**

UNIT V
Advanced Systems and Techniques: -
Wavelength Division Multiplexing, DWDM, optical amplifiers, Optical filters, Integrated optics, Optical Networks : SONET / SDH, Photonic switching, Local Area Networks, Optical Sensors. **Lectures 10, Marks 20**

References:
1. Jonn M. Senior - Optical fiber communication (Principles and Practice), EEE
2. G. Keiser - Optical fiber communication, MH
3. Joseph Palais - Fiber optic communications, Pearson
4. Wilson Hawkes - Opto electronics, PHI
5. Selvrajan, Srinivas - Optical fiber communication, TMH
6. B.P.Pal - Optical fiber systems and sensors
7. Govind P. Agrawal - Fiber optic communications systems, wiley 3rd Ed

List of Practical:
1. Electrical characteristics of (Different type LED)
2. Photometric characteristics of LED / LD (Polar Plot, Intensity Measurement)
3. NA Measurement for Single / Multi de, Gi / S1, fiber
4. Attenuation Measurement of optical fiber
5. Spectral characteristics of LED / LD
6. Fiber optic Analog / Digital transmitter / receiver parameter measurement
7. Study of fiber optical connectors
8. Spectral response of optical fiber
9. Parameter measurement of opto isolator
10. Study of OTDR.

Note: Minimum **EIGHT** practicals are to be performed

W.E.F : 2008- 09

TERM - I
DIGITAL SIGNAL PROCESSING AND PROCESSORS

Teaching scheme: **Examination scheme:**
Lectures: 4 hrs / week   **Theory Paper: 100 Marks (3 Hours)**
Practical: 2 hrs / week   **Practical   :   25 Marks**

UNIT I
Discrete Time Signals and Systems:
Introduction: Basic elements of Digital Signal Processing Systems, Advantage and Limitation of Digital over Analog Signal Processing, Application of Digital Signal Processing: Spectral Analysis, Echo Cancellation, Image Processing, Biomedical Signal Processing, Classification of Signals. Discrete Time Signals: Representation, Standard Discrete Time Signals, Classification of Discrete Time Signals, Simple Manipulations of Discrete Time Signals, Sampling of Analog signals, Aliasing, Sampling Theorem. Discrete Time System: Block diagram representation of Discrete Time Systems, Classification of Discrete Time System, Convolution Sum, Properties of Convolution, Causality and Stability condition in terms of the Impulse Responses. Meaning of IIR, FIR, Recursive, Nonrecursive Systems, and Impulse Response of LTI Recursive System. Cross Correlation and Auto Correlation of two sequences.   **Lectures 10, Marks 20**

UNIT II
Z Transform and its application to the analysis of LTI system:
Definition of Z transform, Meaning of ROC, Properties of ROC, Properties of Z transform, Inverse Z transform, Pole Zero plot of the function, Pole location and time domain behavior for causal sequences. Analysis of LTI Systems in Z domain: The System Function of LTI system, Response of LTI system with zero initial condition, Transient and Steady state responses, Causality and Stability of System. Pole zero cancellation. The one sided Z transform, Response of the system with nonzero initial conditions. Solution of difference Equations using Z transform.   **Lectures 10, Marks 20**

UNIT III
Frequency Analysis of Discrete Time Signals and Systems:
The Fourier Transform of Discrete time Aperiodic Signals and Energy Density Spectrum, Frequency response of Discrete Time Systems, Magnitude and Phase response. Frequency Domain Sampling: The Discrete Fourier Transform, IDFT, The DFT as Linear Transformation, Twiddle factor, Properties of the DFT, Use of DFT in linear filtering, Frequency analysis of signals using DFT. Magnitude spectrum of signals. FFT Algorithms: Radix2 DIT and DIF algorithms to computer DFT and IDFT.   **Lectures 10, Marks 20**

UNIT IV
Design and Realization of Digital Filters:
Basic Network Elements, FIR Filter Structure and Design: Direct form, cascade form, frequency sampling and linear phase structure. Fourier series, Windowing method. Gibbs phenomenon, Frequency sampling method of design. IIR Filter structure and Design: Direct form, Cascade form, Parallel form and Transposed structures. Impulse invariance, Bilinear Transformation method of design.   **Lectures 10, Marks 20**

UNIT V
DSP Architecture:
Architectural features of DSP processors: Multiplier and Multiplier Accumulator (MAC), Modified Bus Structures and Memory Access schemes in DSP, Multiple access memory, Multiport Memory, Pipelining, Special addressing modes, Onchip Peripherals. Different generation of DSP Processors, Fixed point and floating point numeric representation and Arithmetic, Introducing the TI 6000 platform, Features of TMS320C62X Processors, EDMA, Host Port Interface, Expansion Bus, External Memory Interface (EMIF), Boot Loader, McBSP, Interrupts, Timers, Basic Interfacing Techniques.   **Lectures 10, Marks 20**

References:
1. Proakis and Monolakis - Digital Signal Processing-Principles, Algorithms and Applications, Pearson Publication / PHI
2. Mitra S.K. - Digital Signal Processing, TMH Publication
3. B.Venkataramani, M.Bhaskar - Digital Signal Processor, Architecture, Programming and Applications,TMH.
4. Texas Instruments - Technical Reference Manual
5. Teaching Material for TI6000 platform from Texas Instruments
6. Thomas Cavicchi - Digital Signal Processing, Wiley
7. Ingle & Prokis – Digital Signal Processing Using MATLAS, 2nd Ed, Thomson Learning.

List of Practical:
1. Basic operations on sequences of equal and unequal lengths.
2. Sampling of continuous time signal and aliasing effect.
3. Convolution of two sequence\ Impulse response.
4. Spectrum of signals using DFT.
5. Frequency response of LTI Discrete time system.
6. Designing of FIR Filter.
7. Designing of IIR Filter.
8. Sampling audio signal at different sampling rate using DSP kit.
9. Interfacing with DSP Kit.
10. Implementation of digital filter using DSP Kit.
11. Using ADC and DAC for signal acquisition and play back after processing.

Note: Minimum **EIGHT** practicals are to be performed. At least **TWO** on any DSP platform.

W.E.F : 2008- 09

TERM - I
COMPUTER COMMUNICATION NETWORK

Teaching scheme: Examination scheme:
Lectures: 4 hrs / week   Theory Paper: 100 Marks (3 Hours)
                                                                   Term Work   :   25 Marks

UNIT I
Introduction to Computer Network: OSI model, TCP / IP and other network models, Different Networks: Novell Netware, Arpanet, NSFNET, Internet. Network Topologies: LAN, WAN, MAN
Physical Layer: Basic for data communication: Fourier analysis, Bandwidth Limited Signal. Transmission media: Twisted pair, Baseband coaxial cable, Broadband coaxial cable, Fiber optics. Wireless Transmission: Radio transmission, Microwave transmission, Infrared and light wave Transmission. Switching. ISDN: Narrowband ISDN: ISDN services, System architecture, Interface. Broadband ISDN: Virtual switching, Circuit switching, ATM Network, Transmission in ATM networks, ATM switches. Cable TV and internet over cable   **Lectures 10, Marks 20**

UNIT II
Data link layer: Design issues: Framing, Error detection and correction code, Flow control Data Link Protocols: Unrestricted Simplex Protocol, stop and wait protocol, Simplex Protocol for a Noisy Channel. Sliding Window Protocols: One bit sliding window, Using Go-Back n, Protocol using Selective Repeat. Practical Example of Data Link Protocols: The Data Link layer in HDLC, internet, ATM.
Medium access sub layer: Channel allocation Problem: Static Channel and dynamic Channel allocation in LANs and MANs. Multiple Access Protocols: ALOHA, Carrier Sense Multiple Access, Collusion Free Protocols, Wireless LAN Protocols. IEEE Standards For LANS and MANS:IEEE Standard 802.3 and Ethernet, (IEEE Standard 802.4) token Bus, (IEEE Standard 802.5) Token Ring, (IEEE Standard 802.6) distributed Queue Dual Bus. (IEEE Standard 802.2) Logical Link Control.
                                                                                    Lectures 10, Marks 20

UNIT III
Network layer : Design Issue: Internal Organization ,Virtual circuit and Datagram subnets, Routing algorithm: Shortest Path Routing, Flooding, Hierarchical Routing, Broad Cast Routing, Routing for mobile host, Multicast routing, Congestion Control Algorithms: Congestion Prevention Policies, Control in virtual Circuits Subnets, choke Packets, Load Shedding.
                                                                                    Lectures 10, Marks 20

UNIT IV
 Internetworking: The network layer in the internet: IP Protocol, IP Address, Subnet, Internet control Protocols, Internet multicasting, IPv4: Datagram, Fragmentation, Checksum, Options ,IPv6: Advantages, Packets Formats Extension Headers. Address Resolution Protocol (ARP), RARP, DHCP. The Network Layer in the ATM Networks: Routing and Switching, Traffic Shaping, Congestion Control, ATM LANs.
                                                                                    Lectures 10, Marks 20

UNIT V
 Transport layer: The Internet Transport Protocols: TCP: Services, Features, Segments, Connections, Flow control, Error Control, congestion Control, UDP. QOS (Quality of Services) ATM AAL layer protocol.
Application layer: Network security, Domain Name system, SNMP, Electronic Mail; the World Wide Web, Multi media.
                                                                                    Lectures 10, Marks 20

References:
1.   Andrew S Tanebaum - Computer Networks, 4th Ed. PHI/ Pearson education.
2.   Behrouz A Forouzan - Data Communication and Networks, 3rd Ed. TMH.
3.   S. Keshav - An Engineering approact to Computer Networks, 5th Ed. Pearson.
4.   W.A. Shay - Understanding communication and Networks, Thomson.
5.   Irvine Olifer - Computer Networks: Principles, Technology and Protocols, Wiley India.
6.   William Stalling – Data and Computer communications, 7th Ed. PHI

Term Work: It is 50% based on theory and 50% based on minimum FIVE assignments on above syllabus (one assignment for each unit)

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B.E. (ELECTRONICS, ELECTRONICS AND COMMUNICATION, ELECTRONICS AND TELECOMMUNICATION)

W.E.F : 2008- 09

TERM - I

VLSI DESIGN (ELECTIVE I)

Teaching scheme:
Lectures: 4 hrs / week
Practical: 2 hrs / week

Examination scheme:
Theory Paper: 100 Marks (3 Hours)
Practical   :   25 Marks
Term work   :   25 Marks

UNIT I
Introduction:
History of HDL: Brief history of VHDL, brief history of Verilog. Structure of VHDL and Verilog module: Structure of Entity / Module, Port. Operators in VHDL and Verilog: Logical, Relational, Arithmetic Shift and Rotate Operators. Data types of VHDL and Verilog. Types of Architecture use in VHDL and Verilog: Behavioral Description, Structural Description, Switch level Description, Data-flow Description, Mixed-type Description. Simulation and Synthesis and comparison between them.
Lectures 10, Marks 20

UNIT II
Data-flow Description (VHDL / Verilog): Structure of Data-flow Description: Signal declaration and Signal assignment statements, Concurrent Signal assignment statements, Constant declaration and assignment statements, Assigning a delay to the signal assignment statements, VHDL / Verilog Programming using Data-flow description and Common errors occurs during programming.
Behavioral Description (VHDL / Verilog): Structure of Behavioral Description for both VHDL/Verilog. VHDL variable assignment statement. Sequential statements for VHDL / Verilog: IF statement, Signal and variable (only for VHDL) assignment, Case statement, Loop statement. VHDL/ Verilog Programming using Behavioral description and Common errors occur during programming.
Lectures 10, Marks 20

UNIT III
i) Structural Description (VHDL / Verilog): Organization of structural design, Binding, State machines, Generic (VHDL), Parameter (Verilog), VHDL / Verilog Programming using Structural description and Common errors occurs during programming.
ii) Switch Level Description (VHDL / Verilog): Single NMOS and PMOS switches: NMOS and PMOS switch description for VHDL / Verilog, Serial and parallel combinations of switches. Switch level description of: Primitive gates, Combinational logics, Sequential circuits. CMOS switch. Bidirectional switches.
iii) Procedures (VHDL), Task (Verilog) and Functions (VHDL / Verilog)
Lectures 10, Marks 20

UNIT IV
Mixed type Description (VHDL / Verilog): User defined data types in VHDL, VHDL Packages, Implementation of Arrays, and Mixed-type Description Programming.
Advanced HDL Description (VHDL / Verilog): File processing in VHDL / Verilog. VHDL record types. Programming of File processing for VHDL / Verilog.
Architecture of Xilinx 9500 series CPLD.
Lectures 10, Marks 20

UNIT V
Xilinx Spartan 4000 series FPGA.
Testing of Logic Circuits:
Fault model, path sensitizing, random test. Design of testability, BIST (Built in self test), Boundary scan test.
Introduction to various Debugging Tools .Introduction to Simulation Tools.
Introduction to Digital Pattern Generator and Logic Analyser. Advantage of Logic Analyzer with built in Digital Pattern Generator over Simulator.
Lectures 10, Marks 20

References:
1. John F. Wakerly - Digital Design, Principles and Practices, Pentice Hall Publication.
2. Nazeib M. Botros - HDL programming Fundamentals VHDL and Verilog , Thomson.
3. Stephen Brown and Zvonko Vranesic - Fundamentals of Digital Logic with VHDL design, McGraw Hill
4. Douglas Perry - VHDL , Tata MC-Graw Hill
5. Xilinx data manual - The Programmable Logic data Book
6. Sudhakar Yalamanchil - An Introduction to VHDL from Synthesis to Simulation
7. Bhaskar – A VHDL Primer, Pearson
8. Zwolinski – Digital System Design with VHDL, Pearson

List of Practical:

Minimum **EIGHT** practicals on VHDL / Verilog coding, simulation and synthesis with implementation on CPLD / FPGA devices. and test performance using 32 channel pattern generator integrated with logic analyzer apart from verification by simulation with tools . Use the pattern generator to generate input signal and truth tables. (PC Based instruments may also be used)

Simulation, Synthesis, and Implementation and observe Real-time validation using pattern generator and Integrated logic Analyzer**:**

Group A. Combinational Logic: (At least THREE of the following must be covered)

1. Write VHDL code to realize all the logic gates

2. Write a VHDL program for the following combinational designs
   a. 2 to 4 decoder
   b. 8 to 3 (encoder without priority & with priority)
   c. 8 to 1 multiplexer
   d. 4 bit binary to gray converter
   e. Multiplexer, demultiplexer, comparator

3. Write a VHDL code to describe the functions of a Full Adder Using following modeling styles.
4. Write VHDL code to display messages on the given seven segment display and LCD and accepting Hex key pad input data

Group B. Sequential logic: (At least THREE of the following must be covered)

1. Develop the VHDL codes for the following flip-flops,
   SR, D, JK, T.

2. Design 4 bit binary, BCD counters (Synchronous reset and Asynchronous reset) and "any sequence" counters.
3. Implementation of 8 – Bit Left / Right Shift Register.

Group C. Implement 32 bit ALU for any (Arithmetic / Logical) Function.
          (At least ONE of the following must be covered)
Write a model for 32 bit ALU using the schematic diagram shown below.(example only)

A (31:0)   B (31:0)

Opcode (3:0)

Enable

Out
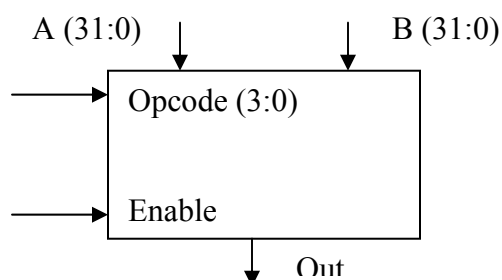
❑ ALU should use combinational logic to calculate an output based on the four bit op-code input
❑ ALU should pass the result to the out bus when enable line in high, and tri-state the out bus when the enable line is low.
❑ ALU should decode the 4 bit op-code according to the given in example below

OPCODE	ALU OPERATION
1.	A + B
2.	A - B
3.	A Complement
4.	A * B
5.	A AND B
6.	A OR B
7.	A NAND B
8.	A XOR B

Group D. INTERFACING (At least Two of the following must be covered)

1. Write VHDL code to control speed, direction of DC and Stepper motor
2. Write VHDL code to accept 8 channel Analog signals, Temperature sensors and display the   data on LCD panel or seven segment displays.
3. Write VHDL code to generate different waveforms (Sine, Square, Triangle, Ramp etc.,) using DAC change the frequency and amplitude.
4. Write VHDL code to simulate Elevator operations
5. Write VHDL code to control external lights using relays.

TERM - I
ROBOTICS (ELECTIVE I)

Teaching scheme:	**Examination scheme:**
Lectures: 4 hrs / week	**Theory Paper: 100 Marks (3 Hours)**
Practical: 2 hrs / week	**Practical : 25 Marks**
	Term work : 25 Marks

UNIT I
Introduction:
Automation and Robotics, Definition, Basic Structure of Robots, Classification of Robots based on co-ordinate system, present trends and future trends in robotics, Overview of robot subsystems, Components of Robot system-Manipulator, Controller, Power conversion UNIT etc, Specifications of robot.   **Lectures 10, Marks 20**

UNIT II
Dynamics and Kinematics:
Dynamic constraints, velocity and acceleration of moving frames, Robotic Mass Distribution and Inertia, Tension, Newton's equation, Euler equation, Dynamic Modeling of Robotic Manipulators, Homogeneous co-ordinate vector operations, matrix operation, co-ordinate reference frames, Homogeneous transformation and manipulator orientation relative points reference frames, forward solutions- Link co-ordinate frames, D-H matrix, Inverse or back solution- problem of obtaining inverse solution, techniques of using direct and geometric approach.   **Lectures 10, Marks 20**

UNIT III
End Effectors and Actuators:
Different types of grippers, vacuum and other methods of gripping, overview of actuators, Internal and External sensors, position, relocking and acceleration sensors, proximity sensors, force sensors, touch slip laser range finder, camera.
                                                                                                   Lectures 10, Marks 20

UNIT IV
Motion Planning and Controllers:
On-off trajectory, relocking and acceleration profile, Cartesian motion of manipulator, joint interpolated control, jacobian in terms of D-H matrix, Obstacle avoidance, Basic control system, control loops of robotic system, Fuzzy controllers.
Robot Vision:
Machine Vision system, description, sensing, Digitizing, Image Processing and Analysis and Application of Machine Vision System, Robotic assembly sensors and Intelligent Sensors. Object recognition.   **Lectures 10, Marks 20**

UNIT – V
Robots for Industrial Automation:
Need for Automation, Robotics for automation. Robot Intelligence and Task Planning, MEMS (Micro Electro Mechanical Systems) – Introduction and working principle, Nano-robots.   **Lectures 10, Marks 20**

References:
1.   Robert J Schilling - Fundamentals of Robotics: Analysis and Control, PHI / Pearson
2.   Klafter, Thomas, Negin - Robotic Engineering, PHI, New Delhi
3.   Yoram Koren - Robotics for Engineers, McGraw Hill, New York
4.   T.C. Manjunath - Fundamentals of Robotics, Nandu Publishers, Mumbai
5.   R. K. Mittal, I. J. Nagrath - Robotics and Control , TMH, New Delhi
6.   HSU - MEMS and Microsystems Design and Manufacture, TMH, New Delhi
7.   John J. Craiz - Introduction to Robotics Mech and control, Pearson 3rd ed

List of Practical:

1) Study of motion conversion (rotary to rotary, rotary to linear) using mechanical components.
2) To build robot arms using mechanical components and applying motor drive.
3) To build robot for given configuration and degrees of freedom.
4) Motion of robot for each degree of freedom. Teaching a sequence to robot using Teach Pendant.
5) To perform pick and place operation using Simulation Control Software.
6) Robot path planning using Simulation and Control Software.
7) Study of Pneumatic Robot OR Study of Robot Vision System.
8) 2D simulation of a 3 D of robot arm. (C / C++ OR MATLAB)
9) Direct Kinematics analysis of 4 - axis robot. (C / C++ OR MARLAB)

Note: Minimum **EIGHT** practicals are to be performed.

W.E.F : 2008- 09

TERM - I
BIOMEDICAL INSTRUMENTATION (ELECTIVE I)

Teaching scheme: **Examination scheme:**
Lectures: 4 hrs / week   **Theory Paper: 100 Marks (3 Hours)**
Practical: 2 hrs / week   **Practical   :   25 Marks**
                                                          Term work   :   25 Marks

UNIT I
Modern Imaging System:
Principles of NMR Imaging systems, Image reconstruction technique, Basic NMR components, biological effects of NMR imaging, Advantages, diagnostic ultrasound, physics of ultrasound waves, Medical ultrasound, Basic Pulse Echo Apparatus, A-scan, M- mode, B-scan, Real time Ultrasonic imaging system, Biological effects of ultrasound, Medical thermography, Physics of thermography, Infrared Detector, pyro-electric vidicon camera etc.   **Lectures 10, Marks 20**

UNIT II
Cardiac Pacemakers and Defibrillators:
Need for pacemakers, external pacemakers, and Implantable pacemakers, recent developments, pacing system analyzer, need for defibrillators, DC defibrillators, Implantable defibrillators, and Defibrillators analyzers. Blood gas analyzers Acid base balance, Blood pH measurement, measurement of blood PCO_2, Blood PO_2 measurement, intra arterial blood gas monitoring, and complete gas analyzers, types of blood cells, coulter counters, and Auto recognition and differential counting of cells.
Lectures 10, Marks 20

UNIT III
Instruments for Surgery:
Principle of surgical diathermy, surgical diathermy machine, safety aspects, surgical diathermy analyzers, LASER, pulsed RUBY laser, Nd - YAG laser, He-Ne laser, Argon laser, CO_2 laser, laser safety, microwave diathermy, ultrasonic therapy unit,, pain relief through electrical simulation.   **Lectures 10, Marks 20**

UNIT IV
Heamo-dialysis Machines and ventilators:
Function of kidneys, Artificial kidney , Dialysers, Membranes for Heamo-dialysis Heamo-dialysis Machine, Portable kidney machine, Mechanics of respiration Artificial ventilation , ventilators Types, ventilator terms, classification of ventilators Modern ventilators, HF ventilators, Humidifiers, Nebulisers and Aspirators.   **Lectures 10, Marks 20**

UNIT V
Biomedical Telemetry and telemedicine:
Introduction, physiological parameters adaptable, wireless telemetry, single channel, Multi-channel, multi–patient telemetry, components of Bio-telemetry system, Implantable telemetry, Transmission of Analog and physiological signals over telephone , Telemedicine. Spectro-photometry, colorimeters, Automated Biochemical analysis. Infusion Pumps, Implantable Infusion systems.   **Lectures 10, Marks 20**

References:
1. Cromwell - Biomedical Instrumentation, Pearson / PHI
2. Khandpur - Handbook of Biomedical Instrumentation
3. Webster - Biomedical Instrumentation, Wiley

List of Practical:

1. Measurement of echo with ultrasound system.
2. Study of Internal Pacemaker.
3. Study of Pacemaker simulator.
4. Measurement of pacing pubes with the pacemaker system.
5. Study of ON - DEMAND pacemaker system
6. Measurement of blood cell count.
7. Study of Surgical diathermy machine.
8. Study of Heamo dialysis Machine
9. Study of Nebulisers.
10. Measurement of Heart beats by wireless telemetry system.
11. Study of Ultrasonic therapy machine.
12. Study of Spectrophotometer.

Note: Minimum **EIGHT** practicals are to be performed

W.E.F : 2008- 09

TERM - I
ARTIFICIAL INTELLIGENCE (ELECTIVE I)

Teaching scheme: **Examination scheme:**
Lectures: 4 hrs / week   **Theory Paper: 100 Marks (3 Hours)**
Practical: 2 hrs / week   **Practical   :   25 Marks**
                                                                     Term work   :   25 Marks

UNIT I
Introduction to Artificial Intelligence:
Definition, AI Problems, physical symbol system and hypothesis, AI Technique, Turing test, Problem as a state space search, production system, Problem characteristics, breadth first search, depth first search, AI representation, Properties of internal Representation, Heuristic search techniques, Best files search, A* and AO* Algorithms, Mean and ends analysis

Lectures 10, Marks 20

UNIT II
Knowledge Representation using Predicate Logic:
Predicate calculus, Predicates and Arguments, ISA hierarchy, Frame notation, Resolution, Natural deduction.
Knowledge Representation using Non-monotonic Logic: TMS (Truth Maintenance System), Statistical and probabilistic reasoning, Fuzzy Logic, Knowledge representation, Semantic Net, Frames, Script, Conceptual dependency.

Lectures 10, Marks 20

UNIT III
Planning: Types of planning, Block world, strips, Implementation using goal stack, Nonlinear planning with goal stacks, Hierarchical planning, List commitment strategy.**Perception:** Action, Robot architecture, Vision, Texture and images, Representing and recognizing scenes, Walzs algorithm, Constraint determination, Trihedral and Nontrihedral figures labeling.

Lectures 10, Marks 20

UNIT IV
Learning: By training neural networks, Introduction to neural networks, Neural net architecture and applications. Natural Language Processing and understanding, Pragmatic, Syntactic, and Semantic analysis, Finite State Machine, ATN, Understanding sentences.

Lectures 10, Marks 20

UNIT V
Expert System: Utilization and functionality, architectures of Expert system, Knowledge representation, Two case studies on expert systems. **Game Playing:** Minimize search procedure, Alpha-beta cutoffs, Waiting for Quiescence, Secondary search.

Lectures 10, Marks 20

References :
1. Eugene Charniak, Drew McDermott - Introduction to Artificial Intelligence
2. Elaine Rich, Kerin Knight - Artificial Intelligence, TMH
3. B. Yegnanarayana - Artificial Neural Network, PHI
4. Dan W. Patterson - Introduction to artificial intelligence and expert system, PHI / Pearson
5. Timothy J Ross - Fuzzy Logic with Engineering Application, TMH

List of Practical:

Assignments based on:

1. Implementation of single perceptron training algorithm.
2. Implementation of fuzzy membership function.
3. Implementation of Unification Algorithm.
4. Hill Climbing Algorithm.
5. Game playing with Min / Max Search.
6. Implementation of Dynamic database.
7. Parsing method implementation.
8. Development of Mini Expert System using Prolog.
9. Application development using Neural Network.
10. Development of Intelligent Perception System.

Note: Minimum **EIGHT** practicals are to be performed.

W.E.F : 2008- 09

TERM - I
PROJECT I

Teaching scheme: **Examination scheme:**
Practicals: 2 hrs / week   **Oral   :   25 Marks**
                                                                                        Term Work   :   25 Marks

1. Every student individually or in a group (group size is of 3 students. However, if project complexity demands a maximum group size of 4 students, (the committee should be convinced about such complexity and scope of the work.) shall take a project in the beginning of the (B.E. first Term) seventh term in consultation with the guide and the project must be completed in the (B.E. Second Term) eighth term.

2. The project proposal must be submitted in the institute in the beginning of the (B.E. first Term) seventh term. While submitting project proposal care is to be taken that project will be completed within the available time of two term i.e 2 Hrs per week for (B.E. first Term) seventh term and 4 Hrs per week for (B.E. Second Term) eighth semester (total time become 12*2 + 12*4 = 72 Hrs per project partner). The final title of the project work should be submitted at the beginning of the (B.E. Second Term) eighth semester.

3. Project title should be precise and clear. Selection and approval of topic:

    Topic should be related to real life application in the field of Electronics and Telecommunication
                                                        OR
    Investigation of the latest development in a specific field of Electronics or Communication or Signal Processing

                                                        OR

    The investigation of practical problem in manufacture and / or testing of electronics or communication equipments

                                                        OR

    The Microprocessor / Microcontroller based applications project is preferable.

                                                        OR

    Software development project related to VHDL, Communication, Instrumentation, Signal Processing and Agriculture Engineering with the justification for techniques used / implemented is accepted.

                                                        OR

    Interdisciplinary projects should be encouraged. The examination will be conducted independently in respective departments.

4. The group should maintain a logbook of activities. It should have entries related to the work done, problems faced, solution evolved etc., duly signed by guide.

5. The group is expected to complete details system design, layout etc. in (B.E. first Term) seventh term, as a part of term work in the form of a joint report. Project report must be submitted in the prescribed format only. No variation in the format will be accepted.

6. One guide will be assigned at the most three project groups.

7. The guides should regularly monitor the progress of the project work.

8. Assessment of the project for award of TW marks shall be done by the guide and a departmental committee (consisting of minimum two teachers with experience more than three years) as per the guidelines given in the following table.

A) ASSESSMENT OF PROJECT I TERMWORK B.E. FIRST TERM

NAME OF THE PROJECT _____
NAME OF THE GUIDE: _____

Sr No	Exam Seat No	Name Of Student Marks	Assessment by guide (70%)					Assessment by Departmental committee (30%)			Grand Total	Out of 25 Marks
			Liter-ature survey	Topic Se le-tion	Docum-entation	Atte-nden-ce	To-tal	Eval-uation (10%)	Pres-ntaion (20%)	Total		
			10	05	15	05	35	05	10	15	50	25

Sign of Guide   Sign. of Committee Members   Sign. of H. O. D.

9. The guide should be internal examiner for oral examination (If experience is greater than three years).

10. The external examiner should be from the related area of the concerned project. He should have minimum of five years of experience at degree level / industry.

11. The evaluation at final oral examination should be done jointly by the internal and external examiners.

B.E. (ELECTRONICS, ELECTRONICS AND COMMUNICATION, ELECTRONICS AND TELECOMMUNICATION)

W.E.F : 2008- 09

TERM - I
SEMINAR

Teaching scheme: **Examination scheme:**
Practical: 2 hrs / week   **Term Work   :   25 Marks**

1. For seminar every student will individually study a topic assigned to him / her and submit a report and shall deliver a short lecture / Seminar on the topic at the end of term.

2. Selection of topic should be done by students in consultation with concerned guide

    a. Topic should be related to branch but it should be extended part of the branch (latest and advance topic).
    b. The topic should be such that the student can gain latest knowledge. Student should preferably refer at least one research paper

3. Seminar topic should not be repeated in the department and registration of the same should be done on first come first served basis

4. Seminar report should be submitted in paper bound copy prepared with computer typing

    a. Size of report depends on advancement of topic.
    b. Student should preferably refer minimum 5 reference books / magazines.
    c. Format of content
        i.   Introduction.
        ii. Literature survey.
        iii. Theory 1) Implementation   2) Methodology
                     3) Application   4) Advantages, Disadvantages.
        iv. Future scope.
        v.   Conclusion.

   5   ASSESSMENT OF SEMINAR for TERM WORK
        Title of seminar: _____
        Name of guide   : _____

Sr. No.	Exam Seat No.	Name of Student	Assessment by examiners					Grand Total
			Topic Selection	Literature Survey	Report Writing	Depth of understanding	Presentation	
			5	5	5	5	5	25

6 . Assessment of Literature survey will be based on
        a.   Collection of material regarding history of the topic.
        b.   Implementation.
        c.   Recent applications.

7. Assessment of Depth of understanding will be based on
        a.   Questioning by examiners.
        b.   Questioning by students.
        c.   What the student understands i.e. conclusion regarding seminar.

8. Assessment of presentation will be based on;
    a.   Presentation time (10 minutes)
    b.   Presentation covered (full or partial)
    c.   Way of presentation
    d.   Questioning and answering (5 minutes)

9. Examiners should be a panel of two one of them must be guide. Examiner must have experience at least 3 years. Examiners will be appointed by HOD in consultation with Principal.

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B.E. (ELECTRONICS ENGINEERING)

W.E.F : 2008- 09

TERM - II
DIGITAL COMMUNICATION SYSTEMS

Teaching scheme: **Examination scheme:**
Lectures: 4 hrs / week   **Theory Paper: 100 Marks (3 Hours)**
Practical: 2 hrs / week   **Practical   :   25 Marks**
                                                                Term work   :   25 Marks

UNIT I
Fourier analysis and Random signal theory. Fourier series and transform, properties, correlation and convolution of signals. Probability Joint and conditional probability. statistical average. Continuous random variables - PDF and statistical averages, random processes stationary .Time average and ergodicity. Mean, moment, variance for different continuous and discrete variables.   **Lectures 10, Marks 20**

UNIT II
Wave form coding. Sampling of signals, natural and flat top samples, PCM systems, quantization, companding S / N ratio DM. ADM DPCM systems. LPC speech synthesis, Digital multiplexing, statistical time division multiplexing, Noise in PCM, Noise in DM, ADM, DPCM.   **Lectures 10, Marks 20**

UNIT III
 Base band data transmission and recovery: Line codes. Base band pulse shaping. Doubinary and M - ary signaling. Base band transmission limitations. ISI, eye diagram, synchronization, scrambler, unscrambler, earty - late synchronization, Integrator and Dump receiver , S / N ratio. Optimum receiver, detection of signal in matched filter, properties of matched filter.
                                                                Lectures 10, Marks 20
UNIT IV
Digital carrier Modulation : Binary ASK, PSK, FSK, schemes. Probability of error, coherent PSK and FSK, DPSK, M – ary PSK, DEPSK, and QPSK.
BFSK, M-ary FSK, Quadrature amplitude modulation probability of error calculation for ASK, PSK, etc. Multi-user access : TDMA, FDMA, CDMA.   **Lectures 10, Marks 20**

UNIT V
Information Theory of coding techniques: Measure of information, Entropy, rate, Shannon's Encoding theorem, mutual information, variable length encoding (Shannon Fano and Hoffman coding), Shannon's theorem on channel capacity. Shannon. Hartley equation for Gaussian channel.
Error detection and correction: FEC and ARQ systems, error correcting and detecting, Block codes, syndrome decoding, Hamming coded, BCH. Codes, convolution codes, CRC.   **Lectures 10, Marks 20**

References:
1. A. B. Carlson - Communication systems ,TMH 4th Ed
2. Siman Haykin - Digital Communication , Wiley 4th Ed
3. B.P.Lathi - Modern Digital and Analog communication systems, Oxford
4. Taub and schilling - Principles of communication system , TMH
5. Singh and Sapre - Communication system Analog and Digital

List of Practicals

1. Verification of sampling theorem. PAM techniques. (Flat top and natural sampling) Effect of variable sampling rate, filter cut off, reconstruction of original signal using filter, aliasing effect
2. Study of DM, ADM, Techniques , observation of effect of slope over load , granular noise and SNR measurement
3. Companded PCM (using A- Law) Plot quantization curve. SNR measurement ,
4. Generation and reception of QPSK in presence of noise
5. Generation and detection of FSK
6. Generation and detection of Quadrature Amplitude shift keying
7. Study of line codes (NRZ, RZ, polar RZ, bi polar (AMI), Manchester) and spectral analysis
8. Generation and detection of DSSS coherent BPSK and spectral analysis.
9. Study of block codes to generate (n, k) code
10. To implement Shannon fano algorithm for variable length encoding (Shannon Fano and Hoffman coding) method using software tool

Note: Minimum **EIGHT** practicals are to be performed

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W.E.F : 2008- 09

TERM - II
POWER ELECTRONICS II

Teaching scheme:
Lectures: 4 hrs / week
Practical: 2 hrs / week

Examination scheme:
Theory Paper: 100 Marks (3 Hours)
Practical   :   25 Marks
Term work   :   25 Marks

UNIT I
Introduction to motor drive: control of motor drives, servo drives, block diagram description, criteria for selecting drive components, match between the motor and the load, match between the motor and the power electronic converter, current rating, voltage rating, switching frequency and the motor inductance, selection of speed and position sensors, servo drive control and current limiting, current limiting in adjustable speed drives.
DC motor drives : block diagram description of DC motor drive, power electronic converter, ripple in armature current, selection of servo drive parameters; line frequency controlled converters, effect of discontinuous armature current, power factor of the line current in adjustable speed drive   **Lectures 10, Marks 20**

UNIT II
Induction motor drives : constant speed drive, adjustable speed drive, block diagram description; speed control for varying stator frequency and voltage, torque speed characteristics, start up considerations, voltage boost required at low frequency, induction motor capability - below and above rated speed, braking in induction motors; harmonic motor currents, harmonic losses, torque pulsation; variable frequency converter classification; variable frequency PWM - VSI drives, adjustable speed control of PWM - VSI drives - speed control circuit and current limiting circuit, induction motor servo drives, variable frequency voltage drives, reduced voltage starting (" soft start ") of induction motor, speed control by static slip power recovery.
Lectures 10, Marks 20

UNIT III
Gate and base drive circuit : preliminary design considerations, dc coupled drive circuits with unipolar output, with bipolar output, optocoupler drive circuits, transformer isolated drive circuits providing both signal and power, cascode drive circuit for normally on power devices, Thyristor drive circuits - gate current pulse requirements gate pulse amplifiers, commutation circuit power device protection in drive circuit, over current protection, blanking times for bridge circuit, "smart" drive circuits for snuberless switching; circuit layout consideration ,minimizing stray inductance in drive circuit - shielding and partitioning of drive circuit, reduction of stray inductance in bus bars, current measurement, capacitor selection aluminum electrolytic capacitors, metalized polypropylene capacitors and ceramic capacitors.   **Lectures 10, Marks 20**

UNIT IV
Snubber circuit : function and types, diode sunbbers, capacitive sunbber, effect of adding a subber resistance, implementation, snubber circuit for thyristors, need for snubber with transistors- turn-off snubber; over voltage snubber, turn-on snubber, snubber for bridge circuit configurations, GTO snubber considerations, component temp control and heat sinks: control of semiconductor device temperature, heat transfer by conduction, thermal resistance; heat sinks; heat transfer by radiation and convection; heat sink ambient calculation.   **Lectures 10, Marks 20**

UNIT V
Power supply and other applicators /   Residential and Industrial application : High frequency fluorescent lighting, Induction heating, Electric welding, High voltage dc transmission, Twelve pulse line frequency converters, Reactive power drawn by converters, rectifier mode of operation, Inverter mode of operation, control of HVDC converters, Harmonic filter and power factor correction, capacitors static VAR cornpensators, Thyristor controlled inductor / Capacitor, converters with minimum energy storage elements, optimizing the utility interface with power electronic systems, generation of current harmonics, harmonics and power factor, harmonic standards and recommended practices, need for improved   utility interface improved single phase utility interface, passive circuits, Active shaping of the input line current.
Lectures 10, Marks 20

References:
1. Ned Mohan, TM Undeland William P. Robbins - Power Electronics converters, Applications and Designs, John Wiley and sons, 2nd Ed.
2. Mohammad M. Rashid - Power Electronics – Circuits, Devices and Applications, PHI, 2nd Ed.
3. M. Rammamoorthy - Introduction to Thyristor and their Applications.
4. Singh and Khanchandani - Power Electronics , TMH, 2nd Ed.

List of Practical:
1. DC drives -2 practical
2. AC drives -2 practical
3. Gate and Base drive – 2 practical
4. Snubber circuit – 2 practical
5. HVDC System - 1 practical
6. Static VAR compensation - 1 practical
7. Industrial heating - 1 practical

Note: Minimum **EIGHT** practicals are to be performed.

W.E.F : 2008- 09

TERM - II
PROCESS INSTRUMENTATION

Teaching scheme: **Examination scheme:**
Lectures: 4 hrs / week   **Theory Paper: 100 Marks (3 Hours)**
Practical: 2 hrs / week   **Term work   :   25 Marks**

UNIT I
Introduction to process control:
Process control principles, Block diagram, control system evaluation, E / P converters , P / E, V / I, I / V, V / F, F / V Converters, Transmitters, 2 wire transmitters, smart transmitters (Wire and wireless). Pneumatic, hydraulic, electric actuators. Control block diagram description: Process measurement, error detector, controller, control element, feedback loop.
Lectures 10, Marks 20

UNIT II
Process Control elements:
Mechanical and Electrical elements, fluid valve, control valve, classification of different parts of a standard control valve, selection of control valve, various types of control valves their characteristics and application , CV noise , Actuators, positioners, cavititation and flashing. Discontinuous controller modes, two position modes, neutral zone, multi position mode, floating control mode, etc.
Lectures 10, Marks 20

UNIT III
Continuous control modes:
Introduction of continuous control modes, P, I, D, PI, PD, PID control , electronic controllers realization of controller modes using op-amp circuits, General features of PID controller, Pneumatic controllers, Hydraulic controllers. Tuning of controllers.
Lectures 10, Marks 20

UNIT IV
Complex control schemes:
 Manual and auto control system, open loop and closed loop system, feedback and feed forward control system, spilt range control, cascade control system and ratio control system , selective and adaptive control. Inverse derivative control, anti reset control, multivariable control, Simple instrumentation schemes for Heat exchanger, Boiler, compressor, distillation column, reactors, dryer, evaporator etc.
Lectures 10, Marks 20

UNIT V
Advance control processes :
Introduction to Computer control process, control computers, basic functions of computer systems, direct digital control, progress in computer control in process industries, unit level control, plant level control, Distributed control system, Supervisory control systems, SCADA system, Data acquisition systems.
Lectures 10, Marks 20

References:
1. Shinskey - process control system, application, design and tuning, MGH
2. Curtis Johnson - Process control Instrumentation technology, JOHN WILEY
3. Liptak - : Hand Book of Process Instrumentation
4. Patranabhis - Process control instrumentation
5. Donald Eckman - Industrial instrumentation , WILEY EASTERN
6. Nagrath gopal - Modern control systems
7. Harriot P - Process control, TMH

List of Practical:

1. Study of Converters: V to F and F to V
2. Study of Wireless Transmitter.
3. To plot characteristics of different valves and calculation of C_v.
4. To study of any one type of discontinuous controller mode.
5. Plotting and calculation of the neutral zone.
6. To study simple instrumentation scheme for distillation column
7. Study of manual and automatic control
8. To study simulation of simple instrumentation scheme for boiler.
9. Study of SCADA system in live plants.

Note: Minimum **EIGHT** practicals are to be performed.

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TERM - II
EMBEDDED SYSTEM (ELECTIVE II)

Teaching scheme:	Examination scheme:
Lectures: 4 hrs / week	Theory Paper: 100 Marks (3 Hours)
Practical: 2 hrs / week	Practical : 25 Marks
	Term work : 25 Marks

UNIT I
Embedded system Introduction:
Introduction to Embedded System, History, Design challenges, optimizing design metrics, time to market, applications of embedded systems and recent trends in embedded systems, embedded design concepts and definitions, memory management, hardware and software design and testing, communication protocols like SPI, SCI, I2C, CAN etc
Lectures 10, Marks 20

UNIT II
System Architecture:
Introduction to ARM core architecture, ARM extension family, instruction set, thumb Instruction set, Pipeline, memory management, Bus architecture, study of on-chip peripherals like I / O ports, timers, counters, interrupts, on-chip ADC, DAC, RTC modules, WDT, PLL, PWM, USB etc. **Lectures 10, Marks 20**

UNIT III
Interfacing and Programming:
Basic embedded C programs for on-chip peripherals studied in system architecture. Need of interfacing, interfacing techniques, interfacing of different displays including Graphic LCD (320X240), interfacing of input devices including touch screen etc, interfacing of output devices like thermal printer etc., embedded communication using CAN and Ethernet, RF modules, GSM modem for AT command study etc. **Lectures 10, Marks 20**

UNIT III
Real Time Operating System Concept:
Architecture of kernel, task scheduler, ISR, Semaphores, mailbox, message queues, pipes, events, timers, memory management, RTOS services in contrast with traditional OS. Introduction to Ucos II RTOS, study of kernel structure of Ucos II, synchronization in Ucos II, Inter-task communication in Ucos II, memory management in Ucos II, porting of RTOS.
Lectures 10, Marks 20

UNIT V
Embedded Linux:
Introduction to the Linux kernel, Configuring and booting the kernel, the root file system, Root file directories, /bin, /lib etc., Linux file systems, Types of file system: Disk, RAM, Flash, Network. Some debug techniques- Syslog and strace, GDB, TCP / IP Networking- Network configuration, Device control from user space- Accessing hardware directly, Multi processing on Linux and Inter Process Communication- Linux process model and IPCs, Multithreading using pThreads - Threads verses Processes and pThreads, Linux and Real-Time Standard kernel problems and patches. **Lectures 10, Marks 20**

References:

1. Rajkamal - Embedded Systems, TMH.
2. David Simon - Embedded systems software primer, Pearson
3. Steve Furber - ARM System-on-Chip Architecture, Pearson
4. Jean J Labrose - MicroC / OS-II, Indian Low Price Edition
5. DR.K.V.K.K. Prasad -   Embedded / real time system, Dreamtech
6. Iyer, Gupta - Embedded real systems Programming , TMH
7. Steve Heath - Embedded System Design , Neuwans

LAB EXERCISE

- Integrated Development Environment Overview (Project creation, down load and debug)
- Study of JTAG Debugger/on-board debugger-emulator.
- ARM Instructions execution (Barrel Shifter, LDR / STR, SMT / LDM**)**

List of Practicals:

GROUP - A
1) Writing basic C-programs for I / O operations
2) C-Program to explore timers / counter
3) C-programs for interrupts
4) Program to demonstrate UART operation

GROUP - B
5) Program to demonstrate I2C Protocol.
6) Program to demonstrate CAN Protocol.

GROUP - C
7) Program to interface LCD
8) Program to interface Keyboard and display key pressed on LCD
9) Program to interface stepper motor

GROUP - D
10) Program to demonstrate RF communication
11) Program to implement AT commands and interface of GSM modem
12) Implementation of USB protocol and transferring data to PC.
13) Implementation of algorithm /program for the microcontroller for low power modes.

uCOS II / Embedded Linux RTOS Examples

GROUP - E
14) Interfacing 4 x 4 matrix keyboards and 16 x 2 characters LCD displays to microcontroller / microprocessor and writing a program using RTOS for displaying a pressed key.
15) Writing a scheduler / working with using RTOS for 4 tasks with priority. The tasks may be keyboard, LCD, LED etc. and porting it on microcontroller/ microprocessor.

GROUP - F
16) Implement a semaphore for any given task switching using RTOS on microcontroller board.
17) Create two tasks, which will print some characters on the serial port, Start the scheduler and observe the behavior.

GROUP – G
18) RTOS based interrupt handling using Embedded Real Time Linux.
19) Program for exploration of (Process creation, Thread creation) using Embedded Real Time Linux.

GROUP – H
20) Program for exploring Message Queues using Embedded Real Time Linux.
21) Ethernet Based Socket Programming using Embedded Real Time Linux.

Note: 1) At least **ONE** practical should be performed from **EACH GROUP**.
2) **TWO** practical should be performed using the **JTAG debugger / on-board Debugger- emulator.**

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TERM - II
DIGITAL IMAGE PROCESSING (ELECTIVE II)

Teaching scheme:	**Examination scheme:**
Lectures: 4 hrs / week	**Theory Paper: 100 Marks (3 Hours)**
Practical: 2 hrs / week	**Practical : 25 Marks**
	Term work : 25 Marks

UNIT I

Digital Image Processing:

Introduction, Examples of Fields that use Digital Image Processing, Fundamental Steps in Digital Image Processing, Components of Image Processing Systems, Image Sensing and Acquisition, Image Sampling and Quantization, Representing Digital Images, Spatial and Gray level Resolution, Basic pixel relationship, Distance Measures, Statistical Properties: Histogram, Mean, Standard Deviation, Introduction to DCT, Walsh, Hadamard, and Wavelet Transform.

Lectures 10, Marks 20

UNIT II

Image Enhancement:

Enhancement in Spatial Domain: Basic Gray Level Transformations, Histogram Processing, Enhancements using arithmetic and logical operations, Basics of Spatial Filtering, Smoothening and Sharpening Spatial filters, Enhancement in Frequency Domain: Smoothening and Sharpening frequency Domain Filters. **Lectures 10, Marks 20**

UNIT III

Image Coding and Compression:

Image Coding Fundamentals, Image Compression Model, Error Free Compression, VLC, Huffman, Arithmetic, RLC, Lossless Predictive Coding; Lossy-Compression, Lossy Predictive Coding, Transform Coding, Discrete Cosine Transform, Image Compression Standards, JPEG Baseline Coder Decoder. **Lectures 10, Marks 20**

UNIT IV

Image Restoration and Color Image Processing:

Image Degradation Model, Noise Models, and Restoration in Presence of Noise in spatial Domain, Linear Filtering, Inverse Filter, Wiener Filter, Constrained Least Square Restoration, Geometric Transformation, Spatial Transformation, and Grey Level Transformation. Color Image Processing, Color Image Fundamentals, Color models, RGB to HIS and vice versa, Color Transforms, Smoothing and Sharpening **Lectures 10, Marks 20**

UNIT V

Image Segmentation:

Image Segmentation: Point, line, Edge detection, Canny Edge Detection, Second Order Derivative, Hough Transform, Thresholding, Region Based Segmentation, Region Growing, Region Splitting and Merging, Image Representation, Chain Codes, Signature, Texture, Use of Principal Component for Description. **Lectures 10, Marks 20**

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References:
1. Gonzalez and Woods - Digital Image Processing, Pearson Education / PHI
2. Arthur Weeks Jr - Fundamentals of Digital Image Processing, PHI.
3. A. K. Jain - Digital Image Processing , PHI
4. Pratt - Digital Image Processing, Wiley
5. Castleman - Digital Image Processing, Pearson

List of Practical:

1. Study of different file formats e.g. BMP, TIFF and extraction of attributes of BMP.
2. Study of statistical properties- mean, standard deviation, profile, variance and Histogram plotting.
3. Histogram equalization and modification of the image.
4. Gray level transformations such as contrast stretching, negative, power law transformation etc.
5. Spatial Domain filtering- smoothing and sharpening filters.
6. DCT / IDCT of given image.
7. Edge detection using Sobel, Prewitt and Roberts operators.
8. Capturing image through grabber card from camera and Process it.
9. Pseudo coloring.
10. Converting color image to B / W image and vice versa
11. Creating noisy image and filtering using MATLAB

Note: Minimum **EIGHT** practicals are to be performed.

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TERM - II

NEURAL NETWORK AND FUZZY SYSTEM (ELECTIVE II)

Teaching scheme:
Lectures: 4 hrs / week
Practical: 2 hrs / week

Examination scheme:
Theory Paper: 100 Marks (3 Hours)
Practical   :   25 Marks
Term work   :   25 Marks

UNIT I
Introduction:
Biological neurons and their artificial model. Models of neuron: McCulloch-pitts Model, Perceptron, Adaline ,Topology: Basic structures of artificial neural network , Basic learning laws: Hebb's law, Perceptron learning law, Widrow and Hoff LMS learning law, Correlation learning law, Instar and Outstar learning law, Learning Methods: Hebbains learning , Competitive learning, Differential competitive learning , Error correction learning, Reinforcement learning, Stochastic learning.

Lectures 10, Marks 20

UNIT II

Perceptron Layer Network:

Perceptron learning Rule. Perceptron architecture: Single neuron Perceptron, Multiple-Neuron perceptron. Training Multiple neuron Perceptron. Limitations of Perceptron.

Supervised Hebbian Learning:

Linear association, Hebbs rule, Performance analysis, Variation of Hebians rule. Performance Surfaces and Optimum points: Taylor's series, Directional derivatives, Necessary condition for Optimality.   **Lectures 10, Marks 20**

UNIT III

Widrow - Hoff Learning:

ADALINE Network, Single ADALINE, Mean square error, LMS algorithm, Analysis of convergence, Adaptive Filtering: Adaptive noise cancellation, Echo cancellation.

Backpropogation Network:

Multilayer Perceptron: Pattern classification, Function approximation. Back propagation algorithm: Performance index, Chain rule, Back propagation the sensitivity.   **Lectures 10, Marks 20**

 UNIT IV

Fuzzy Mathematics:

Classical sets, fuzzy sets, Fuzzy set operations, Procedure of Fuzzy Sets, Crisp Relations, Fuzzy Relations, Operation of Fuzzy Relations , Fuzzy Tolerance and Equivalence Relations membership functions, Defuzzyfication Methods. Manipulation of Linguistic Variables.   **Lectures 10, Marks 20**

UNIT V
Application of Neuro - fuzzy System : Introduction to Neuro **-** Fuzzy System. Types of Neuro – Fuzzy nets, Neuro – Fuzzy Systems Design and implementation.
Fuzzy classification by equivalence relations: C-means clustering, hardening relations from clustering, Fuzzy pattern recognitions. Control applications: Control system design stages, Control Surface, System Identification Problem, Simple Neuro - Fuzzy Logic Controller, Industrial applications.   **Lectures 10, Marks 20**

Reference Books:

1   Fausett - Fundamentals of Neural networks : Architectures, Algorithnors Applications , Pearson
2   B. Yegnanarayana - Artificial Neural Networks, Prentice Hall of India, New Delhi
3   Martin T. Hagan - Neural Network Design , PWS Publishing company (A devision of International Thomson Publishing Inc.)
4   J.M. Zurada - Introduction to Artificial Neural Network, Jaico Publishing House
5   Meherotra Kishan ,Mohan C.K, Ranka Sanjay - Elements Of Artificial   Neural networks, Penram Int Pub, Mumbai.
6   D.E Goldberg , Addision - Genetic Algorithm in Search Optimization and Machine Learning, Wesley Publication
7   Kalyanmoy Deb - Optimization for Engineering Design Algorithms and Examples, Prentice Hall of India ,New Delhi
8   George J. Klir / Bo Yuan - Fuzzy Sets And Fuzzy Logic, Prentice Hall of India, New Delhi / Pearson
9   T. J. Ross - Fuzzy Logic With Engineering Application , McGraw hill Inc. 1995.

Practical: All the Practicals are based on Any Concerns Software.

1. Design and implementation of artificial neural network to compute XOR for two inputs using feedback artificial neural network.
2. Design a perceptron network to solve Classification problem with different classes of input vectors.(Take two or more classes of input vectors)
3. Design the Perceptron model   for pattern recognition. (Take prototype pattern as example)
4. Simulate Adaline algorithm.
5. Implement Back-propagation simulator.
6. Find out the Fuzzy Relation of the given Fuzzy Sets.
7. Verify any one Defuzzification method.
8. Fuzzy pattern recognition.
9. Design any control system using fuzzy logic in simulink

Note: Minimum **EIGHT** practicals are to be performed.

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W.E.F : 2008- 09

TERM - II
NANO –TECHNOLOGY (ELECTIVE II)

Teaching scheme:	**Examination scheme:**
Lectures: 4 hrs / week	**Theory Paper: 100 Marks (3 Hours)**
Practical: 2 hrs / week	**Practical : 25 Marks**
	Term work : 25 Marks

UNIT I
Introduction to physics of solid state, Structure of Energy Bands-Insulators, Semiconductors, conductors, Effective masses, Fermi surfaces, localized Particles-Donors, Acceptors, Deep traps.

Nano, size of matter, different kind of small, Nano Challenges, Fundamental science behind Nanotechnology, Electrons, Atoms, Ions, Molecules, Metals, Other material, Biosystems, Molecular Recognition, Electrical conduction and ohm's law, Quantum Mechanics, Quantum ideas   **Lectures 10, Marks 20**

UNIT II
Investing and manipulating materials in Nano scale, Electron Microscopies, Scanning probes Microscopies, optical Microcopies for nanoscience and technology
Tools for Measuring Nanostructures, Scanning Probe Instrument, Nanoscale Lithography
Tools for measuring Nanostructures, Scanning probe Instrument, Nanoscale Lithograpthy, Dip. Pen. Lithography, E beam Lithogaphfy, Nanosphere Lithographty, Polarizmatization, nanobricks and building Blocks.   **Lectures 10, Marks 20**

UNIT III
Carbon Nano tubes –Synthesis and purification, Filling of Nano tubes, Mechanism of Growth, Electronic Structure, Transport Properties, Mechanical properties, Physical properties, Applications of Nano Tubes such as Field emission and shielding , Computer, Fuel Cell, chemical sensors
Properties of Nanotubes- strength and elasticity, Uses of Nano tubes
Smart Materials, Sensors, nanoscale Bio structure, Energy capture, Transformation and storage, Optics, Electronics, Natural nano scale Sensor, Electromagnetic sensors, Electronics Nose.   **Lectures 10, Marks 20**

UNIT IV
Building blocks digital better, Linking brains with computer, FET to SET fabricating new chips, Quantum wells, wires, Dots - preparation of quantum Nanostructures
Synthesis of Quantum Dots - General strategies, Synthesis in Confined Media, Uses of Nano particles.
Semiconductor Quantum Dots, Synthesis of Quantum dots, Electronic Structure of Nanocrystals   **Lectures 10, Marks 20**

UNIT V
Nanoelectronics – Introduction, The tools of manufacturing of Micro and nanofabrication optical Lithography, Electron Beam lithography, atomic lithography, Quantum Information and quantum computer , How is quantum computer works and difference between the classical computer.
Application in Medical, Understanding how pharmaceutical, Companies develop drug, Delivering new drug Technology, Oil and Water won't help, Mincells, special delivery cancer with Nanoshell.   **Lectures 10, Marks 20**

References:
1. Mark Ratnakar, Daniel Ratnakar – Nanotechnology : A gentle Introduction to Next Big Idea, Prentice hall of India
2. Richard Booker, Eart Boy sen - Nanotechnology Fun and easy way, Wiley
3. Charles P. Poole J.V. Frank J. Owens - Introduction to Nanotechnology , Wiley India ISBN
4. T. Pradeep - Nano: The essentials, understanding Nanoscience and Nanotechnology , TMH
5. Mick Wilson, Kamali Kannangara, Geoff Smith, Michelle Simmons, Burkhard Ragase - NANOTECHNOLOGY basic science and emerging technologies - Overseas press ISBN81 -88689 - 20-3

Note: Minimum **EIGHT** practicals are to be performed, based on above syllabus

NORTH MAHARASHTRA UNIVERSITY JALGAON
B.E. (ELECTRONICS, ELECTRONICS AND COMMUNICATION, ELECTRONICS AND TELECOMMUNICATION)

W.E.F : 2008- 09

TERM - II
INDUSTRIAL VISIT / CASE STUDY

Teaching scheme: NIL   **Examination scheme:**
                                                                                    Term Work   : 25 Marks

EDUCATION TOUR / TECHNICAL VISITS / CASE STUDY AND ITS EVALUATION

1. During (B.E. First Term / Second Term) seventh and / or eighth terms or during vacation between (B.E. First Term / Second Term) seventh and eighth terms, every student; shall visit minimum two industries, factories arranged by colleges and accompanied by teachers. There shall be at least one teacher for a group of 20 students and at least one non-teaching staff accompanied with the students.

2. The colleges should obtain appropriate certificates of visit from the concerned organizations just after the visits.

3. Students should submit written report about the visits individually at the end of (B.E. Second Term) eighth term.

4. The report should contain information about the following points:

    (a) The organization - activities of organization and administrative setup technical personnel and   their main duties.
    (b) The project / industry brief description with sketches and salient technical information.
    (c) The work / processes observed with specification of materials, products, equipments etc. and role of engineers in that organization.
    (d) Suggestions (if any) for improvement in the working of those organizations.

5. The evaluation of the report of technical visits will be made by panel of two teachers appointed by principal based on following points:

    (a) Coverage aspect: All above points should be covered.
    (b) Detailed observations: System / Process / Product explained with data, diagram specifications.
    (c) Quality of presentation: Report should be very objective and should consist of clear and systematic organization of topics and information.
    (d) Viva - voce: A viva -voce shall be conducted on the technical visit report by the teachers to assess the specific knowledge gained by the students for technical applications.

6. The case study should include the study problem in Electronic or in Electronics and telecommunication Engineering branch.

W.E.F : 2008- 09

TERM - II
PROJECT II

Teaching scheme: **Examination scheme:**
Practicals: 4 hrs / week   **Oral   :   50 Marks**
                                                            Term Work :100 Marks

1. The Project group in (B.E. first Term) seventh term will continue the project work in (B.E. Second Term) eighth term and complete project in all respect (assembly, testing, fabrication, tabulation, test result etc.)

2. The group should maintain a logbook of activities. It should have entries related to the work done, problems faced, solution evolved etc., duly signed by guide.

3. The guides should regularly monitor the progress of the project work.

4. The project work along with project report should be submitted as part of term work in (B.E. Second Term) eighth term on or before the last day of the (B.E. Second Term) eighth term

5. Project report must be submitted in the prescribed format only. No variation in the format will be accepted.

6. Assessment of the project for award of TW marks shall be done by the guide and a departmental committee (consisting of minimum two teachers with experience more than three years) as per the guidelines given in the following table.

   B) ASSESSMENT OF PROJECT II TERMWORK (B.E. SECOND TERM)

NAME OF THE PROJECT: _____

NAME OF THE GUIDE: _____

Sr. No	Exam. Seat No	Name Of Students	Assessment by guide (70%)						Assessment by department (30%)			Grand Total
			Fabrication /software / actual work	Executio n of project	Project report	Scope/ Cost / Utility	Attende-nece	Total	Evalu ation (10%)	Prese-ntaion (20%)	Total	
		Marks	20	10	20	10	10	70	10	20	30	100

Sign of Guide   Sign. of Committee Members   Sign. of H. O. D.

7. The guide should be internal examiner for oral examination (If experience is greater than three years).

8. The external examiner should be from the related area of the concerned project. He should have minimum of five years of experience at degree level / industry.

9. The evaluation at final oral examination should be done jointly by the internal and external examiners.

10. The Project work should be kept in department for one academic year after University Examination .