

Seat  
No.

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मधुर - 002

**Digital Techniques and Applications**  
**(143103/183103/233103)**

**P. Pages : 2**

**Time : Three Hours**

**Max. Marks : 80**

Instructions to Candidates :

1. Do not write anything on question paper except Seat No.
2. Answersheet should be written with blue ink only. Graph or diagram should be drawn with the same pen being used for writing paper or black HB pencil.
3. Students should note, no supplement will be provided.
4. Solve **any two** questions from each unit.
5. Figures to right indicate full marks.
6. Use of non programmable calculator is allowed.
7. Draw neat diagram wherever necessary.

**UNIT - I**

1. a) What is sign magnitude representation ? Explain one's complement and Two's complement representation with example. 8
- b) Perform following operations. 8
  - i) Excess 3 addition of 8, 6.
  - ii) Excess 3 subtraction of 8-5.
  - iii)  $(5386.345)_{10}$  to Hexadecimal.
  - iv)  $(125.62)_8$  to binary.
- c) Prove the following using Boolean algebraic theorem. 4
  - i)  $A + \overline{A}B + A\overline{B} = A + B$ . 4
  - ii)  $AB + \overline{A}B + \overline{A}\overline{B} = \overline{A} + B$ .

**UNIT - II**

2. a) Design half subtractor and implement it using NAND gate. 8
- b) Design BCD adder using 4 bit adder IC7483. 8
- c) Design and implement binary to gray code converter. 8

**UNIT - III**

3. a) Draw and explain SR flipflop and JK flipflop with the help of diagram. 8
- b) Draw and explain SISO and PIPO for shift registers. 8
- c) Draw and explain ring counter using D flipflop, also draw its wave form. 8

**UNIT - IV**

4. a) Explain Moore and Melay circuit with help of diagram. 8
- b) Design MOD-5 synchronous counter using JK FF and implement it. Also draw timing diagram. 8
- c) Design and implement decade up counter. 8

**UNIT - V**

5. a) Explain the following parameters. 8
- i) Fan in and fan out.
  - ii) Power dissipation.
  - iii) Noise Margin.
  - iv) Figure of Merit.
- b) Draw and explain CMOS NAND gate and CMOS NOR gate. 8
- c) Draw and explain two input TTL NAND gate with totem pole output. Compare Totem pole and open collector output. 8

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