ELECTIVE - I
VLSI Design
(New) (1251)

P. Pages : 2

Time : Three Hours

Max. Marks : 100

Instructions to Candidates :
1. Do not write anything on question paper except Seat No.
2. Answersheet should be written with blue ink only. Graph or diagram should be drawn with the same pen being used for writing paper or black HB pencil.
3. Students should note, no supplement will be provided.
4. Answer **any two** from each question (unit).
5. Figures to right indicates full marks.
6. Make the question number with specific bit to write answer.
7. Use of non-programmable calculator is allowed.

UNIT - I

1. a) Write the VHDL and verilog HDL codes for 1-bit full adder using data flow description. **10**

    b) Explain the logical operators in VHDL & verilog HDL in detail. **10**

    c) What is the significance of std_logic_1164 ? Explain with example. **10**

UNIT - II

2. a) Explain the procedure and function statements with suitable examples. **10**

    b) Give the syntax rule for If statement and case statement and design JK flip flop using above statements. **10**

    c) Design 4-bit binary to gray code converter using data flow description. **10**

UNIT - III

3. a) Make the VHDL codes for 4-bit full adder using 1-bit full adders with structural description. **10**

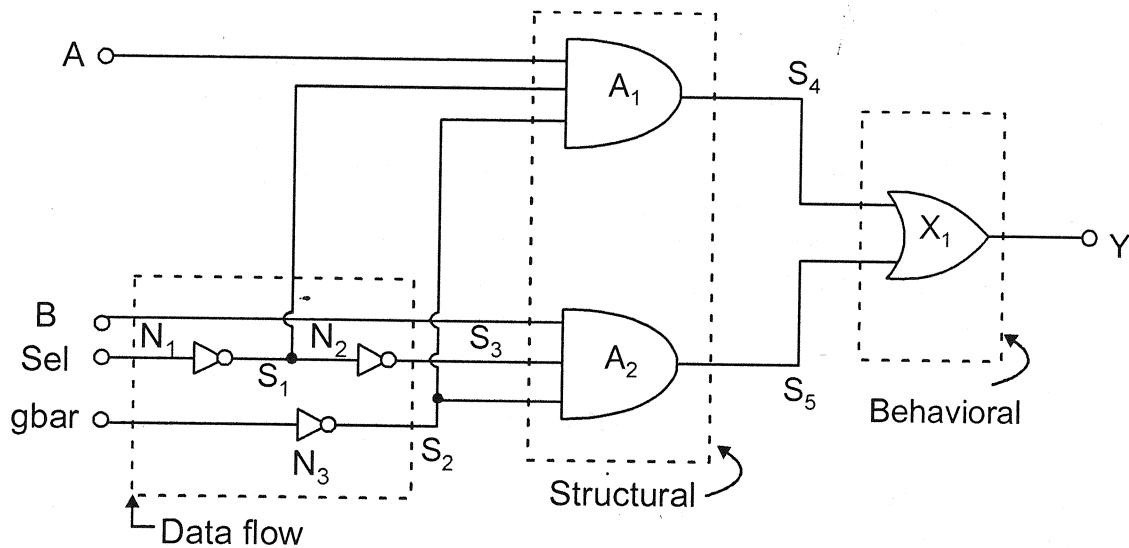   b) Design XOR-gate using switch level description. **10**

c) Enlist the advantages of CMOS and design its VHDL module using switch level description.   **10**

UNIT - IV

4. a) Write the VHDL codes for following circuit using mixed type description as per mention type in fig.   **10**

b) What is record type. Explain with example.   **10**

c) Write the VHDL codes for writing the integer to text file using file processing.   **10**

UNIT - V

5. Write the short notes on :

a) Stuck-at-fault test.   **10**

b) Boundary scan test.   **10**

c) Logic analyzer.   **10**

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