

Seat No.

--	--	--	--	--	--



मानव - 008

Advanced VLSI Design

P. Pages : 2

Time : Three Hours

Max. Marks : 100

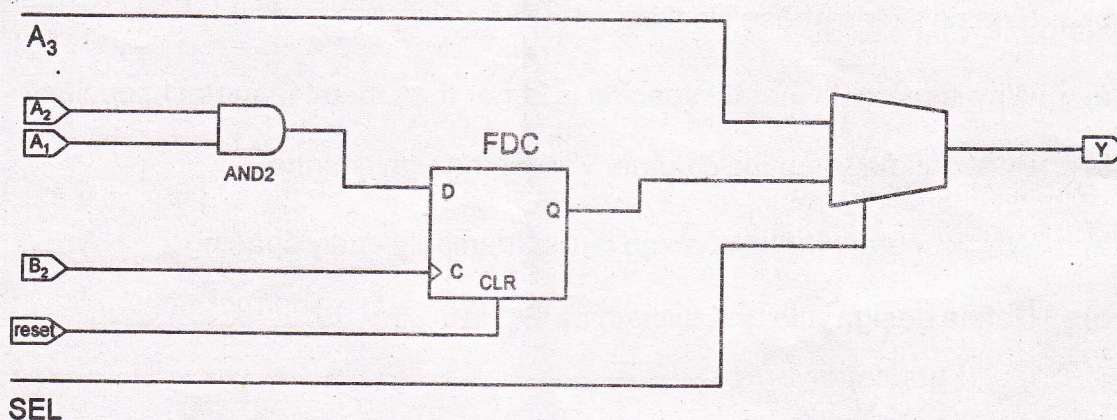
Instructions to Candidates :

1. Do not write anything on question paper except Seat No.
2. Answersheet should be written with blue ink only. Graph or diagram should be drawn with the same pen being used for writing paper or black HB pencil.
3. Students should note, no supplement will be provided.

SECTION - I

1. a) Write VHDL code to infer following RTL :

5



- b) Briefly describe the relationship between these design abstractions :

5

- i) Circuit waveforms vs. digital signals.
- ii) Digital signals vs. binary numbers.

2. a) Draw a stick diagram for the 2 input EX-NOR gate with minimum number of CMOS gates.

5

- b) Design 2 : 1 mux using transmission gate.

5

3. a) Prove that LOW and HIGH transition is $\frac{1}{2}$ to $\frac{1}{3}$ the speed of HIGH to LOW transition ?

5

- b) Plot I_d Vs $V_{ds} = 5V$ for two values of the channel length modulation parameter $\lambda = 0$ and $\lambda = 0.03$. 5
4. a) Differentiate depletion Vs enhancement MOSFET. Which is preferred in CMOS fabrication ? Why ? 5
- b) Differentiate : Delay independent Vs Delay dependent. 5
5. a) Explain the concept of Trench Capacitor. 5
- b) List out problems crop up in driving large loads ? How these are rectified ? 5

SECTION - II

6. a) List the advantages of all carry adders by comparing the average power consumption carried out by them ? Which one is most suitable for low power designs ? 5
- b) Explain single phase clocking rules. 5
7. a) Why is metal2 - metal2 spacing is larger than metal1 - metal1 spacing? 5
- b) Differentiate : Routing channel Vs feedthrough channel. 5
8. a) Why is metal - metal spacing larger than poly - poly spacing ? 5
- b) Define design rule and explain its role in : 5
- i) Fabrication error
- ii) Scalable design.
9. a) Plot the Elmore delay for a metal 2 wire of size $3000\lambda \times 4\lambda$ using 5
- i) 2 sections
- ii) 4 sections
- iii) 8 sections
- b) Why copper is preferred over aluminum as interconnecting material ? 5
10. a) How should tub ties be treated during circuit extraction ? 5
- b) What do you mean by clock skew ? How it can be rectified ? Explain it with neat waveform (s). 5
