

Seat No.

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DFI1344

ELECTIVE - I
VLSI Design
(New) (1254)

P. Pages : 2

Time : Three Hours

Max. Marks : 100

Instructions to Candidates :

1. Do not write anything on question paper except Seat No.
2. Answersheet should be written with blue ink only. Graph or diagram should be drawn with the same pen being used for writing paper or black HB pencil.
3. Students should note, no supplement will be provided.
4. Figures to the right indicate full marks.
5. Assume data wherever necessary.
6. Mark question number with specific bit to write answer.

UNIT - I

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|----|----|---|----|
| 1. | a) | List and explain different styles of description. | 10 |
| | b) | Explain in detail shift and rotate operators in VHDL and verilog. | 10 |
| | c) | Explain Data types in VHDL. | 10 |

UNIT - II

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|----|----|---|----|
| 2. | a) | Write VHDL code of 2x2 magnitude comparator in data flow style of description. | 10 |
| | b) | Write VHDL code of 4-bit down counter with Asynchronous active Low clear in behavioral style. | 10 |
| | c) | Explain signal declaration and assignment statement with example. | 10 |

UNIT - III

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| 3. | a) | Explain following with example. | 10 |
| | | i) Binding Between Entity and Architecture. | |
| | | ii) Binding between library and component. | |
| | b) | Draw switch level logic for X-NOR gate with minimum number of transistors and write switch level description for the same. | 10 |
| | c) | Design a 2-bit synchronous counter using JK flip-flop and write the structural description. | 10 |

UNIT - IV

4. a) What is user defined data types ? Give it's format and explain with example. 10
- b) Write VHDL code for addition of two [5x5] matrices. 10
- c) Write VHDL code for finding the greatest element of an array of (N+1) elements. 10

UNIT - V

5. a) Explain : 10
- i) Design for testability.
- ii) Scan path technique.
- b) Compare CPLD and FPGA. 10
- c) Explain fault module for testing logic circuits. 10
