

Seat
No.

--	--	--	--	--	--



BII1308

Computer Organization (New) (1090)

P. Pages : 2

Time : Three Hours

Max. Marks : 100

Instructions to Candidates :

1. Do not write anything on question paper except Seat No.
2. Answersheet should be written with blue ink only. Graph or diagram should be drawn with the same pen being used for writing paper or black HB pencil.
3. Students should note, no supplement will be provided.
4. Figures to the right indicates full marks.
5. Assume suitable data if necessary.
6. Answer **any two** question from each unit.

UNIT - I

1. Processor P1 is one address processor, P2 is two address processor and P3 is three address processor. Write program for all three processors to perform following functions. 10
 $Z = (A + B) * (C - D)$
2. Explain Expanding opcodes in Detail. 10
3. Explain 68000 Register structure. 10

UNIT - II

4. Perform multiplication by using Booth's Algorithm. 10
i) 20×-25
ii) -13×15
5. Explain non - restoring Division algorithm, with example. 10
6. Represent $(-309.1875)_{10}$ in single precision and double precision format. 10

UNIT - III

7. Explain any one method of Hardwired control unit Design. 10
8. Explain nanoprogrammed computer in detail. 10

9. Define and explain following terms. 10
i) Microinstruction
ii) Microroutine
iii) Emulation.

UNIT - IV

10. If blockset Associative cache of 16KB has 8 set with 8 blocks per set and CPU refers the main memory in the address range 00000H - FFFFFH, Then specify number of bits in the fields TAG, SET and WORD. IF CPU happens to refer main memory at following address, clearly indicate where these will be mapped in cache. 10
i) 12465 H ii) 2389 FH.
11. Explain content addressable memory (CAM) in detail. 10
12. Explain SRAM and DRAM. 10

UNIT - V

13. Discuss RISC and CISC. 10
14. Explain Universal serial Bus (USB) in Detail. 10
15. Explain MULTIBUS in detail. 10
