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DII1358

Advanced Computer Architecture (New) (1310)

P. Pages : 2

Time : Three Hours

Max. Marks : 100

Instructions to Candidates :

1. Do not write anything on question paper except Seat No.
2. Answersheet should be written with blue ink only. Graph or diagram should be drawn with the same pen being used for writing paper or black HB pencil.
3. Students should note, no supplement will be provided.
4. Solve **any two** subquestions from each unit.
5. Assume suitable data if necessary.
6. Figures to the right indicate full marks.
7. Draw diagram whenever necessary.

UNIT - I

1. a) Explain parallel processing mechanism in uniprocessor system. 10
b) A workstation uses a 15-MHz processor with a claimed 10-MIPS rating to execute a given program mix. Assume a one cycle delay for each memory access. 10
 - i) What is the effective CPI of this computer ?
 - ii) Suppose the processor is being upgraded with a 30-MHz clock. However the speed of memory sub-system remains unchanged & two clock cycles are needed per memory access. If 30% of the instruction require one memory access & another 5% require two memory access then what is the effective CPI & MIPS rate of upgraded processor.
- c) Discuss various architectural classification schemes. 10

UNIT - II

2. a) Explain RISC scalar processor & CISC scalar processor in detail. 10
b) Explain the s-access & c-access interleaved memory organizations. 10
c) Consider the execution of a program of 15,000 instruction by a linear pipeline processor with a clock rate of 25 MHz. Assume the instruction pipeline has five stages & that one instruction is issued per clock cycle. 10
 - i) Calculate the speedup factor of this pipeline.
 - ii) Calculate the efficiency & throughput of this pipeline processor.

UNIT - III

3. a) Explain SIMD computer organization in detail. 10
- b) Consider the following reservation table for a four stage pipeline with a clock cycle $T=20$ ns.

	1	2	3	4	5	6
S_1	X					X
S_2		X		X		
S_3			X			
S_4				X	X	

- i) What are the forbidden latencies & the initial collision vector ?
- ii) Draw the state transition diagram.
- iii) Determine the minimum average latency.
- iv) List the no. of simple cycles.
- v) Determine the pipeline throughput. 10
- c) Explain linear & non-linear pipeline processor with the help of space time diagram. 10

UNIT - IV

4. a) Explain loosely coupled & tightly coupled multiprocessor system in detail. 10
- b) Write & explain Synchronous & Asynchronous parallel algorithm ? 10
- c) Discuss various vector access memory schemes. 10

UNIT - V

5. a) Explain data flow computer & give it's various advantages & disadvantages. 10
- b) Discuss various principles of multithreading. 10
- c) Explain various issues in shared variable parallel programming model. 10
